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AN IMPROVED FIFO BASED CONTROLLER CIRCUIT FOR SLAVE DEVICES ATTACHED TO A CPU BUS

Abstract

There is described an improved FIFO based controller (12) for controlling the transfer of data from a CPU, typically a microprocessor, to a slave device (e.g. a SRAM) attached thereto to perform the management of tasks (or transactions). To improve performance, parallel access to the FIFO has been implemented in order to process pipe lined tasks in a shortened time. A task consists of an address (Address) and its associated qualifying bits (ST). The improved controller circuit (12) is comprised of four blocks: a task detection circuit (16), a FIFO controller (12), an innovative task management circuit (18) including the FIFO memory (19) and finally, a slave controller (20). The role of the task detection circuit is to detect valid tasks and inhibiting others. The FIFO controller generates signals to add new tasks in the FIFO memory (ADD TASK) and to clear tasks that have been executed when the data are available on the processor bus (CLEAR TASK). When a valid task is presented in parallel to all the fields of the FIFO memory, it

is stored in the first free field thereof. A valid bit (V) stored in a register (27-x) associated to this field is set to prevent writing a new task therein. In particular, the above circuit is very useful to control a dual port SRAM attached as a slave device to the processor bus of a 750 PowerPC microprocessor.